



NEWS RELEASE

Mentor Graphics Attacks Verification Bottlenecks With New Questa Verification Products

Supports SystemVerilog, VHDL, PSL, and SystemC

WILSONVILLE, Ore., May 16, 2005- Mentor Graphics (Nasdaq: MENT) today announced its new line of Questa™ verification products. The Questa verification products offer built-in support for testbench automation, coverage-driven verification (CDV), assertion-based verification (ABV), and transaction-level modeling (TLM).

This initial release includes two new products: Questa SystemVerilog and Questa Advanced Functional Verification (AFV). Both products utilize a new verification technology, QuestaSim, the first standards-based, single-kernel verification engine that integrates an HDL simulator, a constraint solver, an assertion engine, functional coverage, and a common user interface.

"Every survey indicates that verification remains a huge bottleneck in design cycles, and it's clear that the industry must transition to new verification methodologies to eliminate the bottleneck," stated Robert Hum, vice president and general manager of Mentor Graphics Design Verification and Test division. "With Questa, designers can use the latest language standards and methodologies to find more bugs faster and increase verification productivity."

Standards Are Required For New Verification Methodologies

Over the last two years, several new languages targeted at verification have been standardized. The availability of these languages, SystemVerilog, SystemC and PSL, enables design teams to now move to new methodologies like CDV, ABV or TLM without the risk of getting stuck with proprietary languages or solutions.

According to Cliff Cummings, president of Sunburst Design, Inc. and an industry expert on Verilog and SystemVerilog, "We recognize the importance of SystemVerilog as the standard for system-level verification, which will enable a variety of verification methods throughout the design flow. We believe Mentor's Questa solution will increase the adoption of SystemVerilog for advanced verification."

Questa SystemVerilog Enables Verilog Designers to Move Forward

Questa SystemVerilog incorporates the key components of the emerging IEEE P1800 SystemVerilog standard - design constructs, testbench constructs, assertions and the Direct Programming Interface (DPI) - into a single-kernel verification solution. Verilog users now have a standards-based path to the new verification methodologies ensuring future reuse and design portability. The integrated solution also offers performance and debugging advantages over the multi-tool, multi-language solutions users have to put together today.



Questa AFV Provides True Mixed-Language Verification

Questa AFV provides support for SystemVerilog, VHDL, PSL, and SystemC in a single-kernel verification solution. Targeted at mixed-language flows, Questa AFV enables designers to choose the languages that best address their needs. VHDL users will benefit greatly from tight links to the SystemVerilog verification capabilities for constrained-random testbench generation and functional coverage.

Scalable Verification with Other Mentor Graphics Technologies

The Questa products represent the newest addition to Mentor's Scalable Verification solutions. Questa AFV and Questa SystemVerilog are the first of a series of new verification solutions. Questa products integrate with existing Mentor Graphics products to create customized solutions for specific methodologies. ModelSim® users can easily add Questa functionality with add-on options, and the Seamless®, Advance™ MS, 0-In®, and VStation™ product lines are compatible with the new Questa products.

Product Availability

The Questa AFV platform will ship in Q2 2005. Questa SystemVerilog, will also ship in Q2 2005. Term pricing is available. For pricing information and product details, please call **+49 (0)2151-95301-0** or visit the website at www.trias-mikro.de.

About Mentor Graphics

Mentor Graphics Corporation (Nasdaq: MENT) is a world leader in electronic hardware and software design solutions, providing products, consulting services and award-winning support for the world's most successful electronics and semiconductor companies. Established in 1981, the company reported revenues over the last 12 months of over \$700 million and employs approximately 3,850 people worldwide. Corporate headquarters are located at 8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777; Silicon Valley headquarters are located at 1001 Ridder Park Drive, San Jose, California 95131-2314.

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