

This class is intended to introduce you to the concept of **Assertion based verification**, and also give you the tools to start using the techniques in your design and verification tasks. It covers an introduction to the **PSL** language, so that you are able to write the properties and assertions for your code, and also considers simulating with the assertions using **ModelSim** and its Assertion capabilities. It shows how the Assertion capabilities of **ModelSim** combine with its other aspects to help you debug your design efficiently. The Hands-on labs will reinforce the lectures, providing you with the chance to specify 'real' properties in **PSL**, and experience using the tool to simulate what you have written, under the guidance of our expert instructors.

## Inhalt

- Apply the process of assertion based verification.
- Use the PSL Language including:
  - PSL Layers
  - PSL Flavors
  - Boolean Expressions and operators
  - Sequences (SEREs) and operators
  - Properties, and property operators
  - Directives
  - vunits
  - Some Coding Guidelines
- Compile PSL in ModelSim
- Simulate with PSL in ModelSim including:
  - Use of the Assertion Window
  - Assertion Commands
  - Debugging with assertions, using other ModelSim Windows.
- Write and debug more complex assertions, and use them to verify a design.

Note: Labs are all use VHDL Flavor PSL

## Teilnehmer

- Verification Engineers, FPGA and ASIC Designers
- System Designers who wish to use PSL Assertions as part of their specification of lower level functionality.

## Voraussetzungen

- Basic knowledge of FPGA and ASIC and design techniques and procedures
- Basic knowledge of VHDL (The labs will require PSL to be written in VHDL Flavor PSL)
- Experience using the ModelSim simulator for traditional VHDL dynamic simulation.