



High Level C/C++ Synthesis for FPGAs with CatapultC

Abstract

Increasing design complexity, driven by the demand of getting more functionality into less space and simply by the fact that FPGA technology grows the number of gates per device continually, is one of the biggest challenges in today's FPGA design community. Creating all the required functions can not be achieved by simply coding the hardware in HDL languages, as it used to be in the past, because they are too detailed. A more abstract way of describing functionality is needed.

The workshop High Level C/C++ Synthesis for FPGAs with CatapultC explains how untimed C/C++ algorithmic descriptions for implementation into FPGAs can be written. With simple examples the attendees will learn how the sequential language C/C++ can be used to describe hardware components with their data interfaces.

As the high level synthesis tool we will use CatapultC and understand, how we can explore performance and latency of the description with out changing the code. This will enable us to choose the best implementation for a specific hardware (FPGA) platform and give a good estimation of the data throughput and clock frequency before HDL code has been generated.

Goals

- Understand how to write C code for synthesis with CatapultC
- Understand how data interfaces are described
- Understand how the C code can be verified and the generated HDL code can be cross checked against the original C description.
- Understand how memories can be used
- Understand the impact of loops on the performance
- How an architectural exploration can be done and compared against different architectures in terms of performance and area

Who should attend:

FPGA designers or system level designers who need to get to the next level of abstraction with the functional description of the FPGA and need a quick way into the FPGA hardware.

Prerequisites:

- Knowledge of ANSI C/C++
- VHDL or Verilog knowledge is of advantage but not compulsory
- Knowledge of the principles of FPGA design

Duration:

2 days